IN THE CLAIMS

1. (Previously Presented) A semiconductor device comprising:

a plurality of word lines;

an arbiter configured to receive a first entry signal for entering a first access mode and a second entry signal for entering a second access mode, to determine priority of the first and second access modes, and to generate a first mode trigger signal corresponding to a first entry mode and a second mode trigger corresponding to a second entry mode; and

a signal generating circuit configured to generate an internal operation signal in accordance with at least one of the first mode trigger signal and the second mode trigger signal, wherein the arbiter gives priority to the first access mode when the arbiter receives the first entry signal during the time after the second entry signal is supplied and before a predetermined word line of the plurality of word lines is enabled in the second access mode.

2. (Previously Presented) The semiconductor device according to claim 1, wherein the arbiter determines whether the first entry signal has been supplied within a predetermined period or not in accordance with the internal operation signal.

3. (Previously Presented) The semiconductor device according to claim 1, wherein

the internal operation signal is used as a decision signal indicating whether or not a predetermined word line is enabled in the second access mode.

4. (Previously Presented) The semiconductor device according to claim 1, wherein

the signal generating circuit generates a word-line enable signal for enabling the predetermined word line in the second access mode.

5. (Previously Presented) The semiconductor device according to claim 4, further comprising an address generating circuit that generates an address to be used in the second access mode in accordance with the word-line enable signal.

6. (Original) The semiconductor device according to claim 5, wherein the arbiter generates a state signal indicative of the second access mode in accordance with the second entry signal, and

the address generating circuit generates the address in accordance with the state signal and the word-line enable signal.

7. (Previously Presented) The semiconductor device according to claim 1, wherein the arbiter includes:

a first decision circuit which receives the first entry signal and the second entry signal and determines priority of the first and second access modes,

a second decision circuit that determines whether the first entry signal has been supplied within the predetermined period or not, and

a mode trigger generating circuit that generates the first mode trigger signal in accordance with the determined priority, and

wherein the mode trigger generating circuit generates the first mode trigger signal when the first entry signal is supplied to the second decision circuit within the predetermined period.

8. (Previously Presented) The semiconductor device according to claim 7, wherein the second decision circuit generates a cancel signal to stop execution of the

second access mode when the first entry signal is supplied within the predetermined period.

9. (Previously Presented) The semiconductor device according to claim 8, wherein after generating the cancel signal, the second decision circuit generates the second entry signal again to execute the second access mode after execution of the first access mode.

10. (Previously Presented) The semiconductor device according to claim 1, further including an address generating circuit that generates an address to be used for the second access mode, and

wherein the address generating circuit does not generate the address when the arbiter determines the first access mode has priority.

11. (Previously Presented) The semiconductor device according to claim 1, wherein the arbiter includes a time setting unit that determines whether the first entry signal has been supplied within the predetermined period or not.

12. (Previously Presented) The semiconductor device according to claim 1, further comprising an exclusive test terminal that supplies the second entry signal in a test mode.

13. (Previously Presented) The semiconductor device according to claim 12, wherein

the internal operation signal includes a word-line enable signal to enable a predetermined word line in the second access mode, and

the signal generating circuit suppresses generation of the word-line enable signal in accordance with a test signal.

14. (Previously Presented) The semiconductor device according to claim 12, wherein in the test mode, the signal generating circuit receives the first entry signal and generates the word-line enable signal.

15. (Previously Presented) The semiconductor device according to claim 1, wherein the device has a test mode and further comprises an external terminal to which the second entry signal for the test mode is supplied.

16. (Previously Presented) The semiconductor device according to claim 1, wherein the first access mode corresponds to a read or write operation mode and the second access mode corresponds to a self-refresh operation mode.

17. (Previously Presented) The semiconductor device according to claim 1, wherein

the internal operation signal includes a word-line enable signal for enabling a predetermined word line in the second access mode, and

the predetermined period comprises a period from a point at which the second entry signal is enabled prior to enabling of the first entry signal to a point at which the word-line enable signal is enabled.

18. (Previously Presented) A semiconductor device comprising:

a plurality of word lines and

an arbiter configured to receive a first entry signal for entering a first access mode and a second entry signal for entering a second access mode, to determine priority of the first and second access modes, and to generate a first mode trigger signal corresponding to a first entry mode and a second mode trigger signal corresponding to a second entry mode,

wherein the arbiter gives priority to the first access mode when the arbiter receives the first entry signal during the time after the second entry signal is supplied and before a predetermined word line of the plurality of word lines is enabled in the second access mode.

19. (Previously Presented) The semiconductor device according to claim 18, further comprising a signal generating circuit configured to generate an internal operation signal in accordance with at least one of a first mode trigger signal corresponding to the first entry signal and a second mode trigger signal corresponding to the second entry signal.

20. (Previously Presented) The semiconductor device according to claim 19, wherein

the internal operation signal includes a word-line enable signal for enabling a predetermined word line in the second access mode.

21. (Previously Presented) A method for controlling a semiconductor memory device having a first access mode and a second access mode, the method comprising:

determining priority of the first and second access modes in accordance with a first entry signal for entering the first access mode and a second entry signal for entering the second access mode;

executing the second access mode when the second access mode is determined to have priority;

detecting if the first entry signal has been supplied within a predetermined period after execution of the second access mode has been started and before a

predetermined word line of a plurality of word lines is enabled in the second access mode; and

executing the first access mode by priority over the second access mode when the first entry signal is detected.

22. (Original) The method according to claim 21, wherein the step of executing the first access mode includes stopping execution of the second access mode.

23. (Original) The method according to claim 22, further comprising the step of executing the second access mode after the stopping, and execution of the first access mode.

24. (Previously Presented) The method according to claim 22, further comprising the step of stopping generation of an address of the predetermined word line for the second access mode of the semiconductor memory device if the stopping of execution of the second access mode is performed.

25. (Previously Presented) The method according to claim 21, wherein the first access mode corresponds to a read or write operation mode, and the second access mode corresponds to a self-refresh operation mode.

26. (Original) The method according to claim 21, wherein the predetermined period comprises a period from a point at which execution of the second access mode was started to a point at which a predetermined word line in the semiconductor memory device is enabled in the second access mode.

27. (Original) The method according to claim 26, further comprising the step of setting in the second access mode, a word line address for executing a next second access mode after the predetermined word line is enabled.

28. (Original) The method according to claim 21, wherein the predetermined period comprises a period from a point at which the second access mode was executed to a point at which a word-line enable signal is generated for enabling a predetermined word line in the semiconductor memory device in the second access mode.

29-30. (Canceled)

31. (Previously Presented) A semiconductor device comprising:

a plurality of word lines;

an arbiter configured to receive a first entry signal for entering a first access mode and a second entry signal for entering a second access mode, to determine priority of the first and second access modes, and to generate a first mode trigger signal corresponding to a first entry mode and a second mode trigger signal corresponding to a second entry mode; and

a signal generating circuit configured to generate an internal operation signal in accordance with at least one of the first mode trigger signal and the second mode trigger signal,

wherein the arbiter interrupts the second access mode and gives priority to the first access mode when the arbiter receives the first entry signal before a predetermined word line of the plurality of word lines is enabled in the second access mode and after priority for the second access mode has been determined.

Claim 32. (Previously Presented) A semiconductor device comprising:

an arbiter configured to receive a first entry signal for entering a first access mode and a second entry signal for entering a second access mode, to determine priority of the first and second access modes, and to generate a first mode trigger signal

corresponding to a first entry mode and a second mode trigger signal corresponding to a second entry mode; and

a signal generating circuit configured to generate an internal operation signal in accordance with at least one of the first mode trigger signal and the second mode trigger signal,

an address generating circuit configured to generate an address to be used in the second access mode,

wherein the arbiter gives priority to the first access mode when the arbiter receives the first entry signal before the address generating circuit generates the address to be used in the second access mode and after priority for the second access mode has been determined.

Claim 33. (Previously Presented) The semiconductor device according to claim 1, further comprising a command detector circuit that receives an external command and generates the first entry signal.

Claim 34. (Previously Presented) The semiconductor device according to claim 1, further comprising an internal circuit that generates the second entry signal.

Claim 35 (Previously Presented) The semiconductor device according to claim 1, wherein the first access mode corresponds to an external access operation and the second access mode corresponds to an internal access operation.

Claim 36. (Previously Presented) The semiconductor device according to claim 32, further comprising a command detector circuit that receives an external command and generates the first entry signal.

Claim 37. (Previously Presented) The semiconductor device according to claim 32, further comprising an internal circuit that generates the second entry signal.

Claim 38. (Previously Presented) The semiconductor device according to claim 32, wherein the first access mode corresponds to an external access operation and the second access mode corresponds to an internal access operation.

Claim 39. (Currently Amended) The semiconductor device according to claim 19, wherein ~~the predetermined time is a time when~~ the internal operation signal is generated during the time after the second entry signal is supplied and before a predetermined word line of the plurality of word lines is enabled in the second access mode.

Claim 40. (Currently Amended) The ~~semiconductor device~~ method according to claim 21, wherein the first access mode corresponds to an external access operation and the second access mode corresponds to an internal access operation.